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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,128	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed July 18, 2006 in response to the PTO Office Action mailed May 21, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been canceled, amended or added. Claims 1-44 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5-16 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545) in view of McKenzie (US Patent No. 6,453,398).

For claim 1, Long discloses a system, comprising:

a memory mapping logic configured to provide access to memory locations (a virtual-physical memory mapping device for mapping one or more virtual memory addresses requested by the co-processor into corresponding physical addresses, col. 1, lines 35-38), where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a memory quality assurance logic (memories including logic circuits for functions other than data accessing, col. 1, lines 6-7), where the memory quality assurance logic is configured to:

control copying contents between a first memory location and a second memory location (a memory array including a plurality of pages, one or more processing elements, and internal-external address mapping means; the on-chip processing element copies all the values from a particular good page to a spare page, col. 5, lines 36-37);

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location (the host processor atomically changes the mapping function embodied in the mapping

means, col. 5, lines 44-46; after the mapping is changed, the host processor can continue to read and write locations in the good page, but the actual values that are read and written now come from the spare page, col. 5, lines 50-53); and

initiate memory testing of the first memory location (meanwhile, the processing element runs a test program on the good page, col. 5, lines 53-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate a memory quality assurance logic into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

For claim 3, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. Long further discloses the memory mapping logic includes one or more address translation tables (the virtual-physical memory mapping device further includes a multiple-entry translation lookaside buffer for caching virtual-to-physical address mappings, col. 1, lines 43-45).

For claim 5, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to selectively logically remove the first memory location from a first set of memory by reconfiguring the memory mapping logic, based, at least in

part, on a result from the memory testing of the first memory location (the virtual-physical memory mapping device may include devices for comparing, replacing, singly invalidating and multiply invalidating one or more entries of the translation lookaside buffer, col. 1, lines 47-51).

For claim 6, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with the second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (the translation lookaside buffer is adapted to replace entries therein, col. 1, lines 45-46; the virtual-physical memory mapping device may include devices for comparing, replacing, singly invalidating and multiply invalidating one or more entries of the translation lookaside buffer, col. 1, lines 47-51).

For claim 7, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with another memory location from a first set of memory by reconfiguring the memory mapping logic based, at least in part, on a result from the memory testing of the first memory location (col. 1, lines 47-51).

For claim 8, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the memory quality assurance logic is configured to initiate memory testing of the first memory

location by sending one or more signals to a memory testing logic (at power-on time, the host processor selects memory testing on a control line; the select function configures the processing element to perform memory testing, col. 6, lines 4-7).

For claim 9, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. Long further discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first memory location (par. 0026; fig. 1, items 122, 129).

For claim 10, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the memory quality assurance logic selects the second memory location (after the mapping is changed, the host processor can continue to read and write locations in the good page, but the actual values that are read and written now come from the spare page; meanwhile, the processing element runs the test program on the good page, and when the test completes and there is no anomaly discovered, then the mapping means is reset back to its prior state so that accesses from the host processor go to the actual good page again, col. 5, lines 50-58).

For claim 11, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system

instance to physical memory location relationship data, and a memory reconfiguration data (the processing element writes status information in locations of the memory array indicating, for example, that the test program finished executing, and any additional information to signify errors, col. 6, lines 10-13).

For claim 12, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the memory quality assurance logic being operable connected to the one or more data stores (an internal memory array of pages, an embedded processing element, and internal-external address mapping means connected to each other, col. 3, lines 6-9).

For claim 13, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the second memory location is located in internal memory of the memory mapping logic (col. 3, lines 6-9).

For claim 14, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the second memory location is located in internal memory of the memory quality assurance logic (col. 3, lines 6-9).

For claim 15, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the second memory location is physically connected to the first memory location (col. 3, lines 6-9; fig. 1, items 110-116).

For claim 16, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above. McKenzie further discloses the memory quality assurance logic is configured to select the second memory location (col. 5, lines 50-58).

For claim 29, Long discloses a means to provide access to memory locations (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a processor (one or more processing elements, col. 2, line 42);

a memory operably connected to the processor, where the processor can access the memory (fig. 1, items 110, 120);

a memory mapping logic configured to provide access to memory locations in the memory, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (internal/external address mapping, fig. 1, item 130); and

a memory quality assurance logic operably connected to the memory mapping logic (fig. 1, items 120, 130), where the memory quality assurance logic is configured to:

control copying contents of a first memory location between a second memory location (col. 5, lines 36-37);

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location (col. 5, lines 44-46, 50-53); and

initiate memory testing of the first memory location (col. 5, lines 53-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate these elements into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

For claim 30, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 29 above. McKenzie further discloses the system is embedded in a computer (modules use an industry standard form factor and electrical interface, and therefore can be inserted in any general purpose host computer system, col. 3, lines 31-37).

For claim 31, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 29 above. Long further discloses the system is embedded in an image forming device (a number of co-processors could be utilized to speed up various operations such as the production of graphical images for display or printing out, col. 1, lines 22-24).

For claim 32, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 29 above. McKenzie further discloses the memory quality assurance logic includes one or more data stores configured to store one or

more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (col. 6, lines 10-13).

For claim 33, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 29 above. McKenzie further discloses the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (col. 3, lines 6-9; col. 6, lines 10-13).

For claim 34, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 29 above. Long further discloses a memory location selection logic configured to select the first memory location and the second memory location (interrogating a virtual memory table and mapping one or more virtual memory addresses requested by the co-processor into corresponding physical addresses in the memory of the host processing device, col. 1, lines 61-64).

6. Claims 17-19, 21-25, 28, 37-38 and 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545) in view of McKenzie (US Patent No. 6,453,398) and further in view of Leung et al (US PGPub No. 20050044467).

For claim 17, Long discloses a means to provide access to memory locations (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a method comprising:

selectively copying contents of a first memory location to a second memory location (col. 5, lines 36-37);

logically replacing the first memory location with the second memory location (col. 5, lines 44-46; col. 5, lines 50-53); and

initiating memory testing of the first memory location (col. 5, lines 53-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate a method for logically copying from and replacing a first memory location with a second memory location and initiating testing of the first memory location into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

These combined teachings fail to initiating memory testing of the first memory location without an operating system interaction.

Leung, however, discloses a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016).

Long, McKenzie and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Leung suggests that it would have been desirable to incorporate memory testing that is transparent to an operating system into the combined system of Long and McKenzie because this allows for error-correction in an embedded environment (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

For claim 18, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. McKenzie further discloses access to the contents of the first memory location as copied to the second memory location can continue concurrently with the memory testing (the processing elements can be configured for continuous memory testing, memory filling, block transfer, string matching, and data compression while an external host processor concurrently accesses the memory for data reads and writes, col. 2, lines 55-59).

For claim 19, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. Leung further discloses the memory testing of the first memory location can continue without consuming a non-memory operating system resource (par. 0008).

For claim 21, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. Long further discloses the first memory location is logically replaced by the second memory location by reconfiguring address resolving means (col. 1, lines 45-51).

For claim 22, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. Long further discloses selectively logically removing the first memory location from a first set of memory (col. 1, lines 45-51).

For claim 23, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. These teachings further disclose selectively logically replacing the first memory location with a third memory location, where the first memory location and the third memory location are physically located in the same memory apparatus (Long: col. 1, lines 45-51; McKenzie: col. 3, lines 6-9; fig. 1, items 110-116).

For claim 24, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. McKenzie further discloses providing a report concerning a quality of the first memory location, where the report is based, at least in part, on the testing of the first memory location (col. 6, lines 10-13).

For claim 25, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. McKenzie further discloses storing a quality data associated with the quality of the first memory location, where the quality data is based, at least in part, on the testing of the first memory location (col. 6, lines 10-13).

For claim 28, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. Long further discloses selecting the second memory location to logically replace the first memory location (col. 1, lines 45-51).

For claim 37, Long discloses a means to provide access to memory locations (col. 1, lines 35-38), including a means for selectively logically removing the testable memory location from a set of memory based, at least in part, on a result of testing the testable memory location, where the means for selectively logically removing the testable memory location operates without interacting with an operating system (col. 1, lines 47-51).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses means for logically replacing a testable memory location with a replacement memory location (col. 5, lines 44-46; col. 5, lines 50-53); and

means for testing the testable memory location (col. 5, lines 53-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate a method for logically copying from and replacing a first memory location with a second memory location and initiating testing of the first memory location into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

These combined teachings fail to disclose the means for logically replacing, testing, and selectively logically removing of a testable memory location operates without an operating system interaction.

Leung, however, discloses a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016).

Long, McKenzie and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Leung suggests that it would have been desirable to incorporate memory testing that is transparent to an operating system into the combined system of Long and McKenzie because this allows for error-correction in an embedded environment (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

For claim 38, Long discloses a means to provide access to memory locations (col. 1, lines 35-38) including a programmable memory address resolving logic configured to provide access to the target memory location and the replacement memory location (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a memory location identifying logic configured to identify a target memory location and a replacement memory location (col. 5, lines 50-58); and

a test controlling logic operably connected to the programmable memory address resolving logic, the test controlling logic configured to selectively program the programmable memory address resolving logic to divert memory accesses from the target memory location to the replacement memory location and to initiate testing of the target memory location (McKenzie: fig. 1, items 120, 130; col. 5, lines 44-46, 50-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate identifying target and replacement memory locations and replacing and testing the target memory location into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

These combined teachings fail to disclose the memory location identifying logic, the programmable memory address resolving logic, and the test controlling logic do not consume operating system resources.

Leung, however, discloses a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016).

Long, McKenzie and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Leung suggests that it

would have been desirable to incorporate memory testing that is transparent to an operating system into the combined system of Long and McKenzie because this allows for error-correction in an embedded environment (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

For claim 41, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 38 above. Long further discloses the test controlling logic is also configured to selectively reprogram the programmable memory address resolving logic to stop diverting memory accesses from the target memory location to the replacement memory location (col. 1, lines 47-51).

For claim 42, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 38 above. Long further discloses the test controlling logic is also configured to logically remove the target memory location from a pool of memory available to operating system instances without requiring an operating system instance to halt execution (col. 1, lines 47-51).

For claim 43, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 42 above. Long further discloses the test controlling logic logically removes the target memory location from the pool of memory by reprogramming the programmable memory address resolving logic (col. 1, lines 47-51).

For claim 44, Long discloses a means to provide access to memory locations (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a method comprising:

identifying a test memory location and a mirroring memory location (col. 5, lines 50-58);

mirroring the test memory location to the mirroring memory location (fig. 1, item 130; col. 5, lines 36-37);

selectively reconfiguring memory accessing operations so that memory accesses originating in an operating system instance that are addressed to the test memory location are redirected to the mirroring memory location (col. 5, lines 44-46, 50-53); and

testing the test memory location (col. 5, lines 53-54; Leung: par. 0016).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate identifying, mirroring, and selectively reconfiguring memory accessing operations for a mirroring memory location into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

These combined teachings fail to disclose testing a test memory location without disrupting an operating system instance.

Leung, however, discloses a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016).

Long, McKenzie and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Leung suggests that it would have been desirable to incorporate memory testing that is transparent to an operating system into the combined system of Long and McKenzie because this allows for error-correction in an embedded environment (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

7. Claims 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545) in view of McKenzie (US Patent No. 6,453,398) and further in view of Korhonen (US Patent No. 6,742,148).

For claim 35, Long discloses a means to provide access to memory locations (col. 1, lines 35-38).

Long fails to disclose the remaining claim limitations.

McKenzie, however, discloses a method comprising:

selecting a first memory location to test from a first set of memory (col. 5, lines 50-58);

selectively copying contents of the first memory location to a second memory location (col. 5, lines 36-37);

logically replacing the first memory location with the second memory location (col. 5, lines 44-46; col. 5, lines 50-53); and

initiating testing of the first memory location (col. 5, lines 53-54).

Long and McKenzie are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. McKenzie suggests that it would have been desirable to incorporate a method for selectively logically copying from and replacing a first memory location with a second memory location and initiating testing of the first memory location into the system of Long because this would allow memory to test itself continuously, while simultaneously allowing the values in the memory to be accessed normally by the host processor without affecting the access time (col. 2, lines 32-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long as suggested by McKenzie to incorporate the feature as claimed.

These combined teachings fail to disclose a computer-readable medium storing processor executable instructions operable to perform a method.

Korhonen, however, discloses a method using a test pattern for testing a memory page of a computer system while an operating system is active (col. 3, lines 13-15), where one or more software instructions for storing a test pattern (col. 3, lines 40-41) may, as understood by a person of ordinary skill in the art at the time of the invention, be stored on a computer-readable medium.

Long, McKenzie and Korhonen are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Korhonen

suggests that it would have been desirable to incorporate a computer-readable medium storing instructions into the combined system of Long and McKenzie because this would aid in making memory testing a continuous background task, automatically and accurately detect memory failure and ultimately reduces user down time (col. 4, lines 5-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined system of Long and McKenzie to incorporate the feature as claimed.

For claim 36, the combined teachings of Long, McKenzie and Korhonen disclose the invention as per rejection of claim 35 above. Long further discloses logically replacing the first memory location with the second memory location by reconfiguring address resolving means (col. 1, lines 45-51).

8. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), McKenzie (US Patent No. 6,453,398), Leung et al (US PGPub No. 20050044467) and Nakamura (US Patent No. 6,523,135).

For claim 26, the combined teachings of Long, McKenzie and Leung disclose the invention as per rejection of claim 17 above. These teachings fail to disclose testing the first memory location includes two or more test methods.

Nakamura, however, discloses a built-in self-test circuit for a memory including a test mode controller, abstract; including its own microprocessor for generating test patterns such as column bars, checker board, marching, shifted diagonal test and other test patterns (col. 1, lines 15-18).

Long, McKenzie, Leung and Nakamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Nakamura suggests that it would have been desirable to incorporate two or more test methods into the combined system of Long, McKenzie and Leung because this would help to test substantially all the functions or any desired functions of a memory (col. 2, lines 24-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined system of Long, McKenzie and Leung to incorporate the feature as claimed.

For claim 27, the combined teachings of Long, McKenzie, Leung and Nakamura disclose the invention as per rejection of claims 17 and 26 above. Nakamura further discloses the first memory location can be tested by one or more of, a parity test, an electrical test, a striping test, a marching one test, a marching zero test, and a pattern test (col. 1, lines 15-18).

9. Claims 2 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545) in view of McKenzie (US Patent No. 6,453,398) and further in view of Idleman et al (US Patent No. 5,274,645).

For claim 2, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the memory mapping logic includes a crossbar.

Idleman, however, discloses error correction circuitry can be connected to all memories through a series of multiplexer circuits called crossbar switches (col. 4, lines 13-16).

Long, McKenzie and Idleman are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Idleman suggests that it would have desirable to incorporate crossbar switches into the combined system of Long, McKenzie and Leung because they can be used to decouple failed memories from the system (col. 4, lines 16-17). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

For claim 40, the combined teachings of Long, McKenzie and Idleman disclose the invention as per rejection of claims 2 and 38 above. Idleman further discloses the programmable memory address resolving logic includes one or more of, a crossbar and an address translation table (col. 4, lines 13-16).

10. Claims 4, 20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (US Patent No. 6,393,545), McKenzie (US Patent No. 6,453,398), Leung et al (US PGPub No. 20050044467) and Chauvel et al (US PGPub No. 20040024970).

For claim 4, the combined teachings of Long and McKenzie disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the memory quality assurance logic is configured to select the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

Chauvel, however, discloses a method for managing memory in which replacement algorithms may include, random replacement, round robin replacement, and least recently used replacement (par. 0018).

Long, McKenzie and Chauvel are analogous art in that they are of the same field of endeavor, that is, a method for memory management. Chauvel suggests that it would have been desirable to incorporate such methods for managing memories into the combined system of Long, McKenzie and Leung because this may reduce the number of memory accesses and overall power consumption (abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Long and McKenzie to incorporate the feature as claimed.

For claim 20, the combined teachings of Long, McKenzie, Leung and Chauvel disclose the invention as per rejection of claims 4 and 17 above. Chauvel further discloses identifying the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method (par. 0018).

For claim 39, the combined teachings of Long, McKenzie, Leung and Chauvel disclose the invention as per rejection of claims 4 and 38 above. Chauvel further discloses the memory location identifying logic is configured to identify a target memory location using one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method (par. 0018).

Contact Information

11. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

SCElmore

STEPHEN C. ELMORE
PRIMARY EXAMINER

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